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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/816,817 | 04/05/2004 | Hiroaki Matsui | H-1138 | 2722 |

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| EXAMINER | |
|---|---|
| LE, LANA N | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2618 | |

DATE MAILED: 07/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/816,817 | MATSUI ET AL. | |
| | Examiner | Art Unit | |
| | Lana N. Le | 2618 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) 1-2,5,8 is/are rejected.

7)☒ Claim(s) 3,7 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4, 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Auvray (US 5,564,076) in view of Ratto (US 6,798,844) and further in view of Gard et al (US 7,027,793).

Regarding claim 1, Auvray discloses a communication semiconductor integrated circuit device (fig. 1) comprising:

a signal synthesis circuit (211i, 211Q of modulator 213) for synthesizing the I-signals and Q-signals and local oscillation signals (from 214, 215) to carry out modulation and frequency conversion (col 4, lines 55-63),

wherein a low-pass filter (6A, 6B) is provided between said gain variable amplification circuit (4) and said signal synthesis circuit (col 3, line 63 – col 4, line 2); the communication device being capable of transmission by two or more different modulation methods (col 4, line 64 – col 5, line 13). Auvray does not disclose a gain variable amplification circuit for amplifying I-signals of in-phase component and Q-signals of quadrature component with respect to the fundamental wave. Ratto discloses a gain variable amplification circuit (4; fig. 1) for amplifying I-signals of in-phase

component and Q-signals of quadrature component with respect to fundamental wave. It would have been obvious to one of ordinary skill in the art at the time the invention was made to amplify the I and Q signals in order to correct the phase and amplitude imbalance of the differential signals before modulation. Auvray and Ratto do not disclose a communication semiconductor integrated circuit device comprising the amplifier circuit, the synthesis circuit, and the low pass filter. Gard et al disclose a communication semiconductor integrated circuit device comprising the amplifier circuit, the synthesis circuit, and the low pass filter (fig. 1; col 5, lines 6-7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the transmission components within an IC in order to miniaturize the transmitter for compactness and to reduce the number of chips needed for simplification. Auvray, Ratto, and Gard et al do not specifically disclose the low-pass filter is of second or higher order. However, it is notoriously old and well known in the art to have a second order or higher low pass filter. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have high pass filter in order to obtain sharper frequency characteristics than a single order filter.

Regarding claim 2, Auvray, Ratto, and Gard et al disclose the communication semiconductor integrated circuit device according to claim 1, wherein Gard et al disclose a gain variable amplification circuit (132) is provided in the stage subsequent to said signal synthesis circuit (130). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a variable gain circuit in order to allow adjustment of the gain after the frequency conversion to determine an optimum

output signal level as suggested by Gard et al (col 6, lines 63-67).

Regarding claim 4, Auvray, Ratto, and Gard et al disclose the communication semiconductor integrated circuit device according to claim 1, wherein Auvray discloses an amplification circuit (217) of fixed gain is provided in the stage subsequent to said signal synthesis circuit (fig. 2).

Regarding claim 6, Auvray discloses a communication device comprising: a signal synthesis circuit (211i, 211Q) for synthesizing the amplified I-signals and Q-signals and local oscillation signals (from 214, 215) to carry out modulation and frequency conversion (col 4, lines 55-63),

said communication device being capable of transmission by two or more different modulation methods (col 4, line 64 – col 5, line 13), wherein a low-pass filter is provided before said signal synthesis circuit. Auvray does not disclose a gain variable amplification circuit for amplifying I-signals and Q-signals. Ratto discloses a gain variable amplification circuit (4; fig. 1) for amplifying I-signals and Q-signals (col 5, lines 45-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a variable gain circuit in order to strengthen and correct the gain and amplitude of the baseband signal to the desired signal level before modulation Auvray and Ratto do not disclose a communication semiconductor integrated circuit device comprising the amplifier, modulator, filter and a second gain variable amplification circuit is provided in the stage subsequent to said signal synthesis circuit. Gard et al disclose a communication semiconductor integrated circuit device (fig. 1; col 5, lines 6-7) comprising the amplifier (126), filter (124), modulator (130), and a second

gain variable amplification circuit (132) is provided in the stage subsequent to said signal synthesis circuit (130). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a variable gain circuit after the modulator in order to allow adjustment of the gain after the frequency conversion to determine an optimum output signal level as suggested by Gard et al (col 6, lines 63-67).

Regarding claim 8, Auvray, Ratto, and Gard et al disclose a wireless communication system comprising a communication semiconductor integrated circuit device according to claim 1; where Ratto discloses a signal processing semiconductor integrated circuit (DSP1; fig. 1) which generates said I-signals and Q-signals (I_in, Q_in) supplied to the communication semiconductor integrated circuit device (4-7); and a power amplification circuit (8) which amplifies the power of signals outputted from said communication semiconductor integrated circuit device, wherein a signal (I_in, Q_in to 17) for controlling the gain of said gain variable amplification circuit (4) is supplied from said signal processing semiconductor integrated circuit (17) to said communication semiconductor integrated circuit device (4-7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to generate the I and Q signal from a signal processor and controlling the variable amplifier in order to produce the quadrature signals and correcting the gain of signal level of the I and Q signal before modulation.

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Auvray (US 5,564,076), Ratto (US 6,798,844), Gard et al (US 7,027,793) and further in view of Michaels et al (US 4,549,312).

Regarding claim 5, Auvray, Ratto, and Gard et al disclose the communication semiconductor integrated circuit device according to claim 1, wherein Auvray, Ratto, and Gard et al do not disclose said low-pass filter comprises a plurality of capacitive elements and a switch element connected in series with any of a plurality of the capacitive elements, and the cut-off frequency of the low-pass filter can be changed by turning on/off the switch element. Michaels et al disclose a low-pass filter comprising a plurality of capacitive elements and a switch element connected in series with any of a plurality of the capacitive elements, and the cut-off frequency of the low-pass filter can be changed by turning on/off the switch element (col 2, lines 50-62; col 4, lines 7-11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the switching capacitor element in order to select one of the capacitor elements to filter out the most intense interfering signal as suggested by Michaels et al.

3. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Auvray (US 5,564,076), Ratto (US 6,798,844), Gard et al (US 7,027,793) and further in view of Takano et al (US 2004/0,198,257).

Regarding claim 9, Auvray, Ratto, and Gard et al disclose a wireless communication system comprising a communication semiconductor integrated circuit device according to claim 2; where Ratto discloses a signal processing semiconductor integrated circuit (DSP1; fig. 1) which generates said I-signals and Q-signals (I_in, Q_in) supplied to the communication semiconductor integrated circuit device (4-7); and a power amplification circuit (8) which amplifies the power of signals outputted from said communication semiconductor integrated circuit device, wherein a signal (I_in, Q_in to

17) for controlling the gain of said gain variable amplification circuit (4) is supplied from said signal processing semiconductor integrated circuit (17) to said communication semiconductor integrated circuit device (4-7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to generate the I and Q signal from a signal processor and controlling the variable amplifier in order to produce the quadrature signals and correcting the gain of signal level of the I and Q signal before modulation. Auvray, Ratto, and Gard et al do not disclose a signal for controlling the gain of the second gain variable amplification circuit is supplied from said signal processing semiconductor integrated circuit to said communication semiconductor integrated circuit device. Takano et al disclose a signal for controlling the gain of a gain variable amplification circuit (IVGA) is supplied from said signal processing semiconductor integrated circuit (300) to said communication semiconductor integrated circuit device (100). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a gain control signal from the baseband circuit in order to output a ramping voltage to the variable amplifier to ramp the power of the VGA.

Regarding claim 10, Auvray, Ratto, and Gard et al disclose the wireless communication system according to claim 8, wherein Auvray, Ratto, and Gard et al do not specifically disclose the gain of said power amplification circuit is variable, and a signal for controlling the gain of the power amplification circuit is supplied from said signal processing semiconductor integrated circuit to said power amplification circuit. Takano et al disclose the gain of said power amplification circuit (210) is variable, and a

signal for controlling the gain (VsubAPC) of the power amplification circuit is supplied from said signal processing semiconductor integrated circuit (300) via SW1 to said power amplification circuit (210) fig. 11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the gain of the amplifier variable in order to reduce the power consumption of the power amplifier by adjusting to the proper amount that the power amplifier needs.

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Auvray (US 5,564,076) in view of Ratto (US 6,798,844), Gard et al (US 7,027,793) and further in view of Miyake (US 5,732,334).

Regarding claim 11, Auvray, Ratto, and Gard et al disclose the wireless communication system according to claim 8, wherein Auvray, Ratto, and Gard et al do not disclose a band-pass filter is provided between said signal processing semi-conductor integrated circuit and said power amplification circuit. Miyake discloses a band-pass filter (3) is provided between an inherent signal processing circuit (producing modulated signal 22) and said power amplification circuit (4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a BPF in order to remove the unwanted frequency band before strengthen the transmission signal to reduce noise.

***Allowable Subject Matter***

4. Claims 3 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 3, Auvray, Ratto, and Gard et al disclose the communication semiconductor integrated circuit device according to claim 1, wherein Auvray, Ratto, and Gard et al fail to disclose a second gain variable amplification circuit and an amplification circuit having a limiter function are provided in the stage subsequent to said signal synthesis circuit, and wherein modulated transmission signals having information in the phase component and in the amplitude component are amplified through said second gain variable amplification circuit, and modulated transmission signals having information in the phase component and not having information in the amplitude component are amplified through said amplification circuit having a limiter function.

Regarding claim 7, Auvray, Ratto, and Gard et al disclose the communication semiconductor integrated circuit device according to claim 6, wherein Auvray, Ratto, and Gard et al and the cited prior art fail to disclose a second gain variable amplification circuit and an amplification circuit having a limiter function are provided in the stage subsequent to said signal synthesis circuit, and wherein modulated transmission signals having information in the phase component and in the amplitude component are amplified through said second gain variable amplification circuit, and modulated transmission signals having information in the phase component and not having information in the amplitude component are amplified through said amplification circuit

having a limiter function.

***Conclusion***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lana N. Le whose telephone number is (571) 272-7891. The examiner can normally be reached on M-F 9:30-18:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F. Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

6-26-06

Lana Le

LANA LE
PRIMARY EXAMINER